Camera Prototype Board Testing Log

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# Introduction

The camera prototype board (CPB) is a low-voltage image sensor. During operation, the board is run from a 2.5V supply. This document describes the various observations and problems encountered during testing the various circuits of the CPB to verify that they are functioning correctly.

Table . CPB Pin Descriptions

|  |  |  |  |
| --- | --- | --- | --- |
| **Number** | **Name** | **Pin Type** | **Function/Description** |
| 1 | VSS\_A | Ground | Analogue ground |
| 2 | VDD\_A | VDD | Analogue VDD |
| ~~3~~ | ~~NC~~ | ~~-~~ | ~~No Connection~~ |
| ~~4~~ | ~~NC~~ | ~~-~~ | ~~No Connection~~ |
| 5 | PWDN | Input | Sets Device to Power down Standby Mode |
| ~~6~~ | ~~NC~~ | ~~-~~ | ~~No Connection~~ |
| 7 | VREF | VREF | Internal Voltage Reference (2.3V) Connect to ground using 1μF capacitor |
| 8 | VDD\_C | VDD | Core VDD |
| 9 | VSYNC | Output | Vertical Sync Output |
| 10 | HREF | Output | HFEF Output |
| 11 | PCLK | Output | Pixel Clock Output |
| 12 | VDD\_IO | VDD | I/O VDD |
| 13 | CLK | Input | External Clock |
| ~~14~~ | ~~NC~~ | ~~-~~ | ~~No Connection~~ |
| 15 | RESET | Input | Clears all registers and resets them to their default values. |
| ~~16~~ | ~~NC~~ | ~~-~~ | ~~No Connection~~ |
| 17 | VSS\_D | Ground | Digital Ground |
| 18 | Y7 | Output | Digital video output bit[7] |
| 19 | Y6 | Output | Digital video output bit[6] |
| 20 | Y5 | Output | Digital video output bit[5] |
| 21 | Y4 | Output | Digital video output bit[4] |
| 22 | Y3 | Output | Digital video output bit[3] |
| 23 | Y2 | Output | Digital video output bit[2] |
| 24 | Y1 | Output | Digital video output bit[1] |
| 25 | Y0 | Output | Digital video output bit[0] |
| 26 | SIO\_C | Input | SCCB serial interface clock |
| 27 | SIO\_D | I/O | SCCB serial interface data I/O |
| ~~28~~ | ~~NC~~ | ~~-~~ | ~~No Connection~~ |

# Power Up

Figure . Pin Connection Circuit Diagram



2.5V is supplied to pins 19 and 21 (as detailed in Figure 1), and pins 16, 18, 20, 22, 31 and 32 are connected to ground. The CPB draws a very small current of 0.6μA, as measured using a multimeter in series with the CPB.

Power requirements from the camera documentation file state that it should draw 30μW of power when in standby mode, and 40mW when in active mode – giving an expected active current of 12μA (quite clearly much larger than the measured value).

It is suspected that the CPB may be in standby mode, and information relating to the PWDN pin is researched.

It is noted that pin 5 on the camera chip relates to pin 10 on the J1 connector shown in Figure 1. This runs through resistor R1 on the CPB, and the circuit diagram in the documentation claims “R1 = 10 Ω. This is not needed.”

# Suspend Circuit – PWDN Mode

Figure . PWDN Circuit Diagram



Figure 2. shows the circuit diagram for switching between standby and active mode. The transistor flicks the slave device to either PWDN or VDD depending on the potential it receives from the master device. Here, the master device is equivalent to the payload board, and the slave device to the camera board.

When PWDN\_ is driven at 1 (high), the transistor ensures that the PWDN on the slave is driven at 0 (low). This causes active mode. The reverse happens when PWDN\_ is driven at logical 0.

# Alternative Power Up

The CPB has five connection “holes”, two of which are labelled J3 and J4. On the circuit diagram in the documentation, it is shown that J3 and J4 link directly to the VDD and earth pins on the camera chip, suggesting that if an appropriate voltage was driven through J3 and J4 connected to ground, the camera could be powered up without using the pins on the J1 connector.

To test the amplitude of the potential required to power up through J3, the CPB should be connected to a PC using the USB interface and a probe used to record the operating potential across J3.

# Operational Temperature Range

According to documentation, the CPB will only operate between -10 and 70°C, and stable operation is between 0 and 50°C. Initially this was suspected to be problematic, but as the average temperature of the satellite will be approximately 20°C, there is no problem.

# PC Testing

The CPB is connected to a laptop using the USB interface board. Output pins on the J1 connector are probed and their potential characteristics viewed on an oscilloscope. The results can be seen in Table 2.

Table . Oscilloscope observations across J1.

|  |  |  |  |
| --- | --- | --- | --- |
| **Pin No.** | **Voltage** | **Pin No.** | **Voltage** |
| 1 | 2.5 Digital | 17 | 2.5 Digital |
| 2 | 2.5 Digital | 18 | Ground |
| 3 | 2.5 Digital | 19 | 2.5V Steady |
| 4 | 2.5 Digital | 20 | 3V Digital |
| 5 | 2.5 Digital | 21 | 2.5V Steady |
| 6 | 2.5 Digital | 22 | Ground |
| 7 | 2.5 Digital | 23 | NC |
| 8 | 2.5 Digital | 24 | NC |
| 9 | Ground | 25 | NC |
| 10 | NC | 26 | NC |
| 11 | NC | 27 | NC |
| 12 | NC | 28 | NC |
| 13 | 2.5V Steady | 29 | NC |
| 14 | 3V Steady | 30 | NC |
| 15 | Ground | 31 | Ground |
| 16 | Ground | 32 | Ground |

There are unexpected readings from pins 9 and 15. Pin 15 is high at the beginning of every frame.

The probe is then used to measure the potential across the holes on the CPB, as detailed in Table 3.

Table . Oscilloscope observations across J2 through J6.

|  |  |
| --- | --- |
| **Test Post Number** | **Voltage** |
| J2 | NC |
| J3 (labeled 3.3V) | 2.5V |
| J4 | Ground |
| J5 | 3V |
| J6 | 3V |

Next, a logic analyzer is connected to the probes on the CPB. Pin 1 (Y0) shows data of pictures being taken on the screen, with a typical time between transitions of 160ns for 1 bit.

The probes are connected to other output pins with observations as recorded in Table 4.

Table . Logic analyzer observations for a sample of output pins.

|  |  |  |
| --- | --- | --- |
| **Pin #** | **Observed** | **Diagram** |
| 13 | Expected data for the HFEF pin.  |  |
| 15 | Observed typical VSYNC data |  |
| 13 | High at all times |  |
| 15 | Spikes |  |
| 17 | PCLK – Half the time to transmit 1 bit |  |
| 18 | Low at all times |  |
| 14 | SIO\_1 – GND at all times |  |

Pin 13 gave an unexpected result.

# What’s next?

Test pin 13 with the logic analyzer again to clear up the confusion seen in Table 4.

Power up the camera without using the USB interface and make observations of the output pins using an oscilloscope and a logic analyzer. If similar observations are made, talks with OBDH can begin regarding “talking” with the camera and taking photographs.